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(71) Applicant: HEWLETT-PACKARD COMPANY
3000 Hanover Street
Palo Alto,
California 94304-1181 (US)

(72) Inventor: Davidson, Mark N.
2307 Floral Way
Santa Rosa, CA 95403 (US)
Inventor: Hillstrom, Timothy L.
11506-21st Place NE
Lake Stevens, WA 98258 (US)

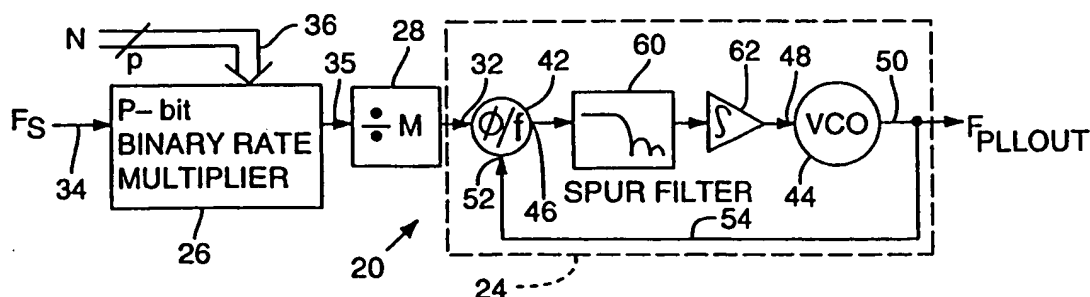
(74) Representative: Colgan, Stephen James et al
CARPMAELS & RANSFORD
43 Bloomsbury Square
London WC1A 2RA (GB)

(54) Phased locked loop synthesizer using a digital rate multiplier reference circuit.

(57) A phase locked loop synthesizer (20) for generating a digitally programmable, continuous wave signal comprises a rate multiplier (26) and divider (28) connected in a reference signal path to a phase detector (42). The rate multiplier and divider generate a reference signal which is programmable to any of a set of regularly spaced frequencies having exact decimal representations. The divider limits the

peak-to-peak phase deviation of the rate multiplier. The phase detector locks a synthesized signal generated by a variable frequency oscillator (44) to the phase of the programmed reference signal. A spur filter (60) connected to the phase detector output (46) reduces spurious frequencies in the phase detector output.

FIG. 1



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EP 95 30 0129

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| Place of search THE HAGUE | | Date of completion of the search 13 September 1995 | Examiner Balbinot, H |
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